REMARKS

Claims 1-15, 17-20, 22-28, and 30-33 were pending. Claims 1, 3, 7-8, 14, 19-20, 22-23, 26-28, and 31 have been amended to clarify the nature of the presently claimed invention. Claims 37-38 have been added. Amendments to claims 7 and 27 are supported by at least paragraphs 59-60 of the Description. Accordingly, claims 1-15, 17-20, 22-28, and 30-39 remain pending subsequent entry of the present amendment.

Allowable Subject Matter

In the present Office Action, claims 32-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Claim 32 and 34 have been rewritten in independent form as claims 37 and 38, respectively, and are in condition for allowance.

35 U.S.C. § 103 Rejections

Claims 1-3, 10, 23, 28, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (patent No. 5,115,506) in view of Sato (patent No. 5,459,682). Claims 1-4, 7-9, 14, 15, 20, 22, 23, 26-28, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin (patent No. 6,154,832) in view of Sato. Claims 10-13, 24, and 25 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin in view of Sato. Claims 5, 6, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin and Sato as applied to claims 1-4, 14, and 15 above, and further in view of M. Morris Mano (book entitled "Computer System Architecture"), hereinafter referred to as "Mano". Applicant respectfully traverses these rejections and requests reconsideration in view of the following remarks.

In paragraph 15 of the present Office Action, the following is suggested regarding claim 7 and 14:

> "Maupin taught mapping logic comprising a plurality of programmable fields, each corresponding to one of a plurality of exception vectors, each of the plurality of fields containing data referencing one of the plurality of shadow register sets (e.g., see col. 5, lines 34-55). Maupin did not expressly detail the shadow mapping logic comprises a plurality of entries, each of which is programmable to associate exception vectors with at least one of the plurality of shadow register sets. However, Sato taught storing in a data memory register select data that is used to by a register set selector to select which register set would be used when a particular interrupt occurred (e.g., see col. 3, lines 2-32), and an interrupt memory (63) to store the content of the select data memory (44) where the data used to select the register set for a particular interrupt can be changed using register set select change enable data stored in program memory along with vector data (51) (e.g., see col. 4, lines 4-37). As to the plurality of entries it would have been obvious to one of ordinary skill that since Sato taught plurality of interrupts (e.g., see fig. 3 and col. 4, lines 20-43) and storing data for determining which register set (e.g., see fig. 1 and col. 3, line 5-37) was to be accessed during the interrupts then the Sato system would have contained plural entries for the plural interrupts (e.g., see fig.3). This register set selector along with the select data memory and interrupt memory and program memory that stored vector data [that related to a leading address of the an interrupt service routine see col. 3, lines 17-26], register set select change data and register select change enable data that is selectively addressed for altering which register set is accessed during any particular interrupt of plural interrupts in the Sato system provides for the claimed mapping logic and interrupt generator. Further as to the type of memory i.e. registers that stored claimed data) One of ordinary skill would have been motivated at the time of the claimed invention to utilize high speed memory (i.e., registers to facilitate the real-time interrupt processing and register set changes as taught by Sato (e.g., see 2, lines 7-27) and take advantage of the reduced cost of memory at the time of claimed invention versus at the time Sato patent was filed."

However, Applicant submits that prior claims 7 and 14 recite features neither taught nor suggested by the cited art. For example, prior claim 7, reproduced below for reference purposes, recited:

> "The processing system as recited in claim 1 wherein said shadow set mapping logic further comprises: a plurality of programmable fields, each corresponding to one of a plurality of exception vectors, each of said plurality of fields containing data referencing one of said plurality of shadow register sets."

It is noted that each of the plurality of fields contains data referencing one of said shadow register sets. Applicant submits that Sato discloses no such features. In contrast, Sato merely discloses a program memory that stores data that that may be added to a current register select data in order to produce information indicating a register set to be selected at the time of an interrupt. More specifically, Sato discloses:

> "The select data memory 44 (a first memory means) stores a PSW indicating the status of the main program. This PSW includes register-set select data 42 indicating which register-set should be selected, and flag data 43 indicating a carry or the like resulting from various operations.
>
> An interrupt memory 63 stores the content of the select data memory 44 which has been used during the main program processing at the time of the interrupt.
>
> A program memory 54 (a second memory means) stores vector data 51, register-set select data change data 52 and register-set select change enable data 53. Of these data, the vector data 51 relates to a leading address of an interrupt service routine. The register-set select data change data 52 indicates data to be added to the register-set select data 42 described later, and is used to obtain information indicating a register-set to be selected at the time of the interrupt. The register set select change enable data 53 indicates permission or denial of the change of the register-set select data 42." (Sato, col. 3, lines 8-26).

As be seen from the above, Sato's register-set select data change data 52 is merely an increment/offset value to be added to the register-set select data 42 to determine which register to be selected at the time of the interrupt. However, register-set select data change data 52 does not contain data referencing one of the shadow register sets, or any register set. There is no reference to one of the register sets until further computation takes place outside of Sato's program memory 54. Accordingly, Applicant finds no teaching or suggestion in Sato of "a plurality of programmable fields, each corresponding to one of a plurality of exception vectors, each of said plurality of fields containing data referencing one of said plurality of shadow register sets," as is recited in prior claim 7.

Applicant has amended claim 1 to incorporate features of prior claim 7 as discussed above. Accordingly, Applicant submits that amended claim 1 is patentably distinguished from the cited art, taken either singly or in combination. Claim 14 has been amended to more closely recite features similar to those of claim 7. Claims 20, 23, 26, 28, and 31 have been amended to include the features of claim 7. For similar reasons, claims 14, 20, 23, 26, 28, and 31 are patentably distinguished as well. Likewise, as each of dependent claims 2-13, 15, 17-19, 22, 24, 25, 27, 30, and 32-39 includes the features of the independent claims upon which it depends, each of claims 2-13, 15, 17-19, 22, 24, 25, 27, 30, and 32-39 is believed patentable for at least the reasons above as well.

In addition, Applicant submits that the dependent claims recite further features neither taught nor suggested by the cited art. For example, claim 3, as amended, recites:

> "The processing system as recited in claim 1 wherein said shadow set mapping logic comprises a map register that binds each of said shadow register sets to particular exception vectors."

It is noted that the recited map register binds each shadow register set to particular exception vectors. These features or not found in any of the cited art. For example, Sato teaches that register-set select data change data 52 is added to the register-set select data 42 to determine which register to be selected at the time of the interrupt. There is no binding in Sato's system between an exception vector and a register set. Rather, a register set to be used in Sato is determined dynamically at the time of an interrupt based upon the above discussed computation. Consequently, exception vectors in Sato are not bound to a particular register set. On the contrary, Sato's system is designed to distribute use of the register sets amongst interrupts and not bind them as is recited in the claim. Additionally, Maupin teaches that each register set is dedicated to a different interrupt source. Interrupt sources are not the same as exception vectors, since an exception vector may be utilized in response to an interrupt from any of a number of different interrupt sources. Nor are these features found in Cohen, wherein there are only two register sets and a determination of which register set to use when an interrupt occurs depends on at least which register set is currently in use. Accordingly, Applicant finds no teaching or

suggestion in any of the cited art, taken either singly or in combination, of "a map register that binds each of said shadow register sets to particular exception vectors," as is recited in amended claim 3. For at least this additional reason, Applicant submits that amended claim 3 is patentably distinguished from the cited art. As claims 19, 22, and 26 recite features similar to those of claim 3, claims 19, 22, and 26 are patentably distinguished as well.

In addition to the above, claim 7 recites the additional features "wherein a contents of each of said plurality of entries is provided by a programmer." These features or not found in any of the cited art. Applicant submits that amended claim 7 is patentably distinguished from the cited art for at least these additional reasons. As claim 27 includes features similar to that of claim 3, claims 27 is patentably distinguished as well.

For at least the above reasons, Applicant submits that each of the claims is patentable over the cited art, either singly or in combination. Accordingly, Applicant believes the application to be in condition for allowance.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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Date: 5/7/2007